ACS APPLIED ELECTRONIC MATERIALS

pubs.acs.org/acsaelm Article

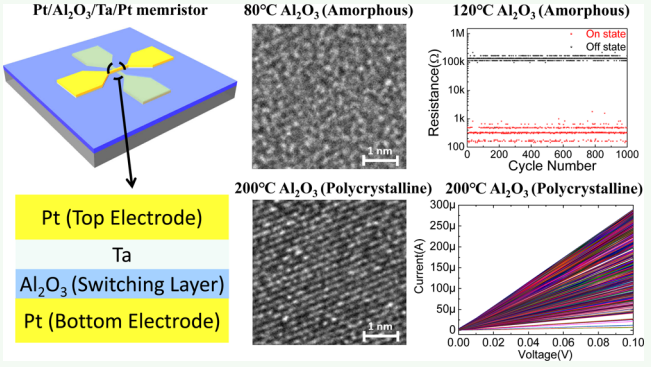
Memristive Device Characteristics Engineering by Controlling the Crystallinity of Switching Layer Materials

Hao Yang, Buyun Chen, Boxiang Song, Deming Meng, Subodh Tiwari, Aravind Krishnamoorthy, Xiaodong Yan, Zerui Liu, Yunxiang Wang, Pan Hu, Tse-Hsien Ou, Paulo Branicio, Rajiv Kalia, Aiichiro Nakano, Priya Vashishta, Fanxin Liu, Han Wang, and Wei Wu*

Cite This: *ACS Appl. Electron. Mater.* 2020, 2, 1529−1537 Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Memristive devices (i.e., memristors) can be highly beneficial in many emerging applications that may play important roles in the future generations of electronic systems, such as bio-inspired neuromorphic computing, high density nonvolatile memory, and field programmable gate arrays. Therefore, the memristor characteristics (such as operation voltage, on/off ratio, and the number of conductance states) must be engineered carefully for different applications. Here, we demonstrate a method to modify the memristor characteristics specifically by controlling the crystallinity of the switching layer material. Through setting the temperature of atomic layer deposition, the crystallinity of deposited Al_2O_3 can be controlled. Using different crystalline Al_2O_3 as the memristor switching layer, the characteristics of the corresponding $Pt/Al_2O_3/Ta/Pt$ cross-point memristors can be modified precisely. The high *I-V* linearity, high on/off ratio (around 10^8), low pulse operation voltage (2.5 V), and multilevel conductance states (314 states) of the $Pt/Al_2O_3/Ta/Pt$ cross-point memristor are demonstrated. More importantly, the mechanism behind this phenomenon is studied. This work deepens our understanding of the working mechanism of memristors and paves the way for using memristors in a broad spectrum of applications.



KEYWORDS: *memristive device, memristor, ReRAM, atomic layer deposition, crystallinity*

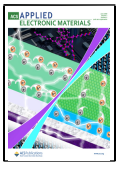
1. INTRODUCTION

Recently, the development of memristive device (i.e. memristor)[1−8] has attracted great interest in the semiconductor industry. Significant progresses have been made in memristive device development,[9,10] including its integration with the Si CMOS circuit,[11,12] switching cycles up to 10^{12},[13] switching speed down to 100 ps,[14] and retention time up to a few years.[15] So far, most efforts are targeting at bio-inspired neuromorphic computing applications.[9,16,17] There are also many emerging applications that can greatly benefit from memristors.[10,18,19] For example, the density of memristors can go beyond 100G bits/cm^2, which is several times higher than currently progressive flash memory technologies.[20,21] Also, the switching power consumption for memristors can be 20 times smaller than that of flash.[20] Moreover, by using memristors as the reconfiguration bits in a field programmable gate array (FPGA), the FPGA is expected to achieve a 5.18× area saving, a 2.28× speedup, and a 1.63× power saving.[22]

However, there are still many critical challenges to be resolved before using memristors in those applications. Different applications have different requirements for the characteristics of memristors, including the operation voltage, the on/off ratio, and the number of conductance states.[23−30] Therefore, significant effort is still needed to tailor the existing memristor technologies for specific applications. The traditional method to engineer memristor characteristics is by selecting appropriate material stack and film thicknesses for both the switching and contact layers,[31] which cannot satisfy all needed requirements.

In this article, we report a method to modify the memristor characteristics specifically by controlling the crystallinity of the switching layer material. Al_2O_3 was used in our $Pt/Al_2O_3/Ta/Pt$ cross-point memristor as the switching layer material. By controlling the atomic layer deposition (ALD) temperature, the crystallinity of Al_2O_3 changed from amorphous to polycrystalline, which affected the memristor performance directly. Through choosing an appropriate Al_2O_3 deposition temperature, the $Pt/Al_2O_3/Ta/Pt$ cross-point memristor can

Received: February 24, 2020
Accepted: May 4, 2020
Published: May 5, 2020



https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537

have great characteristics, such as good $I-V$ linearity, high on/off ratio (around 10^8), low pulse operation voltage (2.5 V), and multilevel conductance states (314 states). The mechanism of modifying memristor characteristics by controlling switching layer crystallinity was also studied.

2. RESULTS AND DISCUSSION

2.1. Device Fabrication. The fabrication process of the Pt/Al_2O_3/Ta/Pt cross-point memristor is shown in Figure 1a.

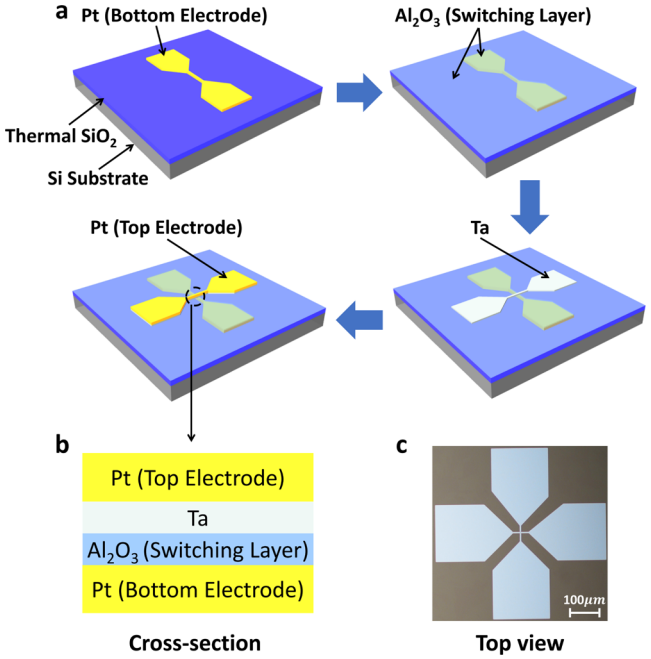


Figure 1. Pt/Al_2O_3/Ta/Pt cross-point memristor. (a) Fabrication process. (b) Schematic of the Pt/Al_2O_3/Ta/Pt cross-point memristor. (c) Optical microscope image of the fabricated Pt/Al_2O_3/Ta/Pt cross-point memristor.

A Si wafer that has 150 nm thermally grown SiO_2 on top was used as the substrate. First, the bottom electrodes were patterned using ultraviolet photolithography. Then, 2 nm Ti (adhesion layer) and 20 nm Pt (bottom electrode metal) were deposited using the electron-beam evaporator, followed by a lift-off process. Next, an 8 nm Al_2O_3 blanket layer was deposited by ALD as the memristor switching layer. The reason that ALD was chosen to deposit the switching layer material is that the ALD temperature can be set precisely (80, 120, 160, or 200 °C) to control the crystallinity of deposited Al_2O_3.[32,33] The details are given in the next section. Finally, 8 nm thick Ta and a 20 nm thick Pt top electrode were defined by a second photolithography, evaporation and lift-off process to get the Pt/Al_2O_3/Ta/Pt cross-point memristor. Figure 1b shows the schematic of the Pt/Al_2O_3/Ta/Pt cross-point memristor, which has a four-layer structure. The optical microscope image of the fabricated Pt/Al_2O_3/Ta/Pt cross-point memristor is shown in Figure 1c.

2.2. Controlling the Crystallinity of the Switching Layer Material. ALD is a chemical vapor deposition technique based on successive, separated, and self-terminating gas–solid reactions of typically two gaseous reactants.[32] Similar to other thin film deposition techniques, the ALD temperature affects the crystallinity of the deposited material.[32,33] The deposited material undergoes transition from amorphous to polycrystalline forms at a characteristic temperature. Al_2O_3 can be deposited by ALD using water (H_2O) and trimethylaluminum as precursors. To compare the crystallinity of Al_2O_3 films at different deposition temperatures, Al_2O_3 (around 16 nm) was deposited for 200 cycles on the Si substrate at four different temperatures (80, 120, 160, and 200 °C), separately.

The refractive indexes of these four Al_2O_3 films were measured using an ellipsometer. With an increase in deposition temperature, the Al_2O_3 refractive index is increased, as shown in Table 1. The data indicate that the Al_2O_3 deposited at higher temperature is denser. The corresponding X-ray diffraction (XRD) spectra of Al_2O_3 films at these four different deposition temperatures are shown in Figure 2a. The Al_2O_3 films deposited at 80 and 120 °C do not have characteristic peaks in the XRD spectra, while the Al_2O_3 films deposited at 160 and 200 °C have clear characteristic peaks in the XRD spectra. These indicate that the Al_2O_3 films deposited at 80 and 120 °C are amorphous, while the Al_2O_3 films deposited at 160 and 200 °C are polycrystalline. According to the Scherrer equation $\tau = \frac{K\lambda}{\beta \cos\theta}$ (where τ is the average grain size, K is a dimensionless shape factor, λ is the X-ray wavelength, β is the line broadening at half the maximum intensity, and θ is the Bragg angle), the estimated average grain size of polycrystalline Al_2O_3 can be calculated, as shown in Table 1. The average grain size of polycrystalline Al_2O_3 is also increased with the increase in the deposition temperature (Table 1), which is consistent with the change in the refractive index.

Table 1. Refractive Index, Crystallinity, and Average Grain Size of Al_2O_3 Deposited at Different Temperatures

Al_2O_3 deposition temperature (°C)	refractive index (λ = 532 nm)	crystallinity	average grain size
80	1.630	amorphous	N/A
120	1.647	amorphous	N/A
160	1.652	polycrystalline	~150.5 nm
200	1.656	polycrystalline	~207.0 nm

Figure 2b–e shows the transmission electron microscopy (TEM) images of Al_2O_3 films deposited at 80 and 200 °C, and the corresponding FFT patterns, respectively. The high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDS) images of the deposited Al_2O_3 film can be found in the Supporting Information Figure. S1. These clearly indicate that the Al_2O_3 film deposited at 80 °C is amorphous, while the Al_2O_3 film deposited at 200 °C is polycrystalline. This direct evidence demonstrates that the deposited Al_2O_3 film has transition from the amorphous to polycrystalline form with increasing deposition temperature. Above all, the crystallinity of the deposited Al_2O_3 can be controlled through the ALD temperature.

2.3. Electrical Performance Characterization. Figure 3a shows the typical bipolar resistive switching $I-V$ curves of the 5 by 5 μm^2 Pt/Al_2O_3/Ta/Pt cross-point memristors, which use Al_2O_3 films deposited at different temperatures (80, 120, 160, and 200 °C) as the switching layer. The memristors can be switched from the off state (high resistance state) to the on state (low resistance state) after positive voltages (V_{set}) are applied.[1,34,35] By sweeping the negative bias (V_{reset}), the memristors can be switched from the on state to the off state, which is defined as the reset process. As shown in Figure 3a, the set and reset voltage of the Pt/Al_2O_3/Ta/Pt memristor is

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529–1537

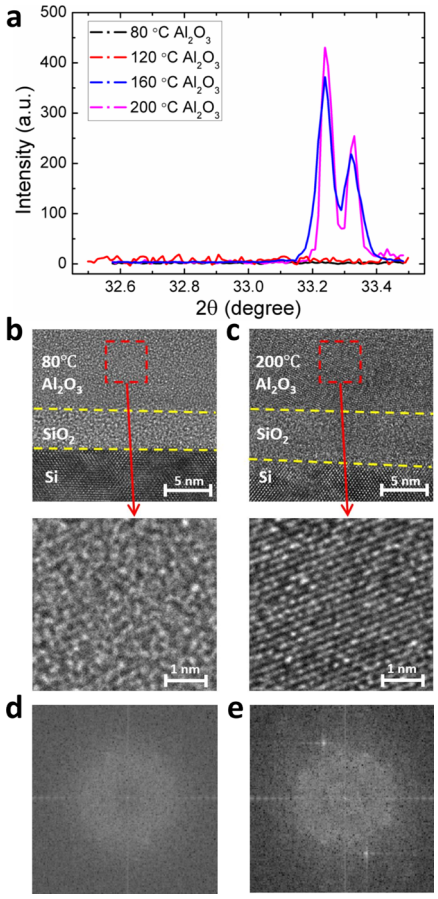


Figure 2. Controlling the crystallinity of Al_2O_3 by changing the ALD temperature. (a) XRD spectra of Al_2O_3 films at different deposition temperatures (80, 120, 160, and 200 °C). (b) TEM image of the 80 °C-deposited Al_2O_3 film, which is amorphous. The SiO_2 layer is the native oxide layer on top of the Si substrate. (c) TEM image of the 200 °C-deposited Al_2O_3 film, which is polycrystalline. The SiO_2 layer is the native oxide layer on top of the Si substrate. (d) Corresponding FFT pattern of the TEM image in (b) (frequency range dc ≈ 1/0.020 [1/nm]). (e) Corresponding FFT pattern of the TEM image in (c) (frequency range dc ≈ 1/0.020 [1/nm]).

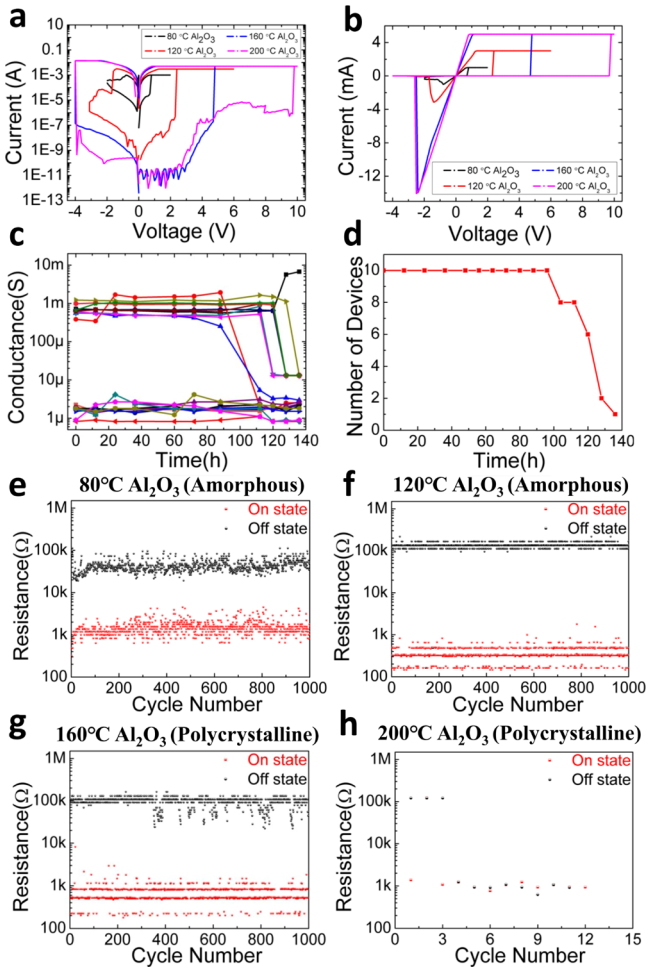


Figure 3. Electrical characteristics of the Pt/Al_2O_3/Ta/Pt cross-point memristor. (a) *I*–*V* curves (plot in log scale) from 5 by 5 μm^2 Pt/Al_2O_3/Ta/Pt cross-point memristors, which use Al_2O_3 films deposited at different temperatures (80, 120, 160, and 200 °C) as the switching layer. The memristors can be set with a positive voltage sweep and then reset with a negative voltage sweep. In the positive voltage sweep, the applied compliance currents for 80, 120, 160, and 200 °C deposited Al_2O_3 memristors of 3, 3, 5, and 5 mA, respectively. (b) *I*–*V* curves (plot in the linear scale, same data as Figure 3a) from 5 by 5 μm^2 Pt/Al_2O_3/Ta/Pt cross-point memristors. The memristors have good *I*–*V* linearity. (c) Retention test of Pt/80 °C deposited Al_2O_3/Ta/Pt cross-point memristors. A total of 20 memristors were used to test the retention. Before the test, 10 memristors were set to on state, and the other 10 memristors were set to off state. (d) Number of the unchanged (did not change from on state to off state) Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor in the 85 °C retention test with respect to the test time. (e) Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor can be repeatedly switched between on and off states with 3 μs pulses (positive pulse voltage: 2.5 V; negative pulse voltage: −2.5 V). Here, the 1000 switching cycle result is shown. (f) 1000 switching cycles of the Pt/120 °C-deposited Al_2O_3/Ta/Pt memristor with 3 μs pulses (positive pulse voltage: 2.5 V; negative pulse voltage: −2.5 V). (g) 1000 switching cycles of the Pt/160 °C-deposited Al_2O_3/Ta/Pt memristor with 3 μs pulses (Positive pulse voltage: 3.4 V; Negative pulse voltage: −3.0 V). (h) Pulse switching of the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor with 3 μs pulses (positive pulse voltage: 6.0 V; Negative pulse voltage: −6.0 V). This device is hard to switch with pulses (switching cycles <10).

increased with the increase in the Al_2O_3 deposition temperature, which is discussed in the next section. Figure 3b shows the linear plot of resistive switching *I*–*V* curves of the Pt/Al_2O_3/Ta/Pt memristors using Al_2O_3 deposited at different temperatures, which demonstrates that our memristors have good *I*–*V* linearity.[16] *I*–*V* curves of multiple switching cycles of the Pt/Al_2O_3/Ta/Pt memristor can be found in the Supporting Information Figure S2. Using the Pt/80 °C-deposited Al_2O_3/Ta/Pt cross-point memristor as the example, the retention characteristic of our memristors was investigated (Figure 3c,d). The result indicates that the memristors are highly stable in each state without degradation over 90 h at the elevated temperature (85 °C). After 90 h, the memristors in the on state started to change to the off state.

The pulse switching measurements of the Pt/Al_2O_3/Ta/Pt memristors that use Al_2O_3 at different deposition temperatures (80, 120, 160, and 200 °C) are shown in Figure 3e–h, respectively. The length of the pulse is 3 μs. More pulse switching data of the Pt/Al_2O_3/Ta/Pt memristor from different devices can be found in the Supporting Information Figures S3 and S4. To compare the difference of Pt/Al_2O_3/Ta/Pt memristors using Al_2O_3 deposited at different temperatures, 1000 switching cycles were done for Pt/80 °C-deposited Al_2O_3/Ta/Pt memristors, Pt/120 °C-deposited

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537

Al_2O_3/Ta/Pt memristors, and Pt/160 °C-deposited Al_2O_3/Ta/Pt. It is noticeable that the used pulse voltage was not very high (±2.5 V for 80 °C-deposited Al_2O_3 and the 120 °C-deposited Al_2O_3 memristor, +3.4 and −3.0 V for the 120 °C-deposited Al_2O_3 memristor, and ±6.0 V for the 200 °C-deposited Al_2O_3 memristor). This is because the memristors were not switched off totally in the pulse switching measurements. This can be demonstrated by observing the on/off ratio (<10^4) in the pulse switching measurements. The on/off ratio in the pulse switching measurements is much smaller than the on/off ratio in the $I-V$ curves (Figure 3a). In addition, for Pt/200 °C-deposited Al_2O_3/Ta/Pt memristors, though ±6 V pulses were used, the memristor was still hard to switch. As a result, the results of only several switching cycles (<10) are shown in Figure 3h. It is noteworthy that the pulse switching results of different memristors are very different, like resistance distribution (variation). The details and the reason behind the differences in pulse switching results are also introduced in the next section.

The number of conductance states is critical to memristors, which is an important feature for bio-inspired neuromorphic computing.[16,36,37] Figure 4a and 4b show the $I-V$ curves for the Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor and the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor with different conductance states, respectively. The Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor can provide conductance ranging from 70 to 350 μS, and the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor can provide conductance ranging from 70 to 2900 μS. Moreover, Figure 4a,b also indicate that our memristors have good $I-V$ linearity. Through controlling the compliance currents, the memristor can be set to the target state precisely, as shown in Figure 4c. The standard deviation of setting the memristor to an exact conductance state is 9 μS. As a result, the Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor can provide 31 states (around 2^5). The Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor can provide 314 states (more than 2^8), which is much better than the Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor. The reason behind this is explained in the next section. Also, the feedback of the memristor programming can help set each memristor to the target state, which ensures the repeatability of conductance state programing. Moreover, the multilevel conductance states of our Pt/Al_2O_3/Ta/Pt memristors are stable (more information can be found in the Supporting Information Figure. S5).

2.4. Working Mechanism Study. As mentioned above, the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor can provide many more conductance states than the Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor can. Additionally, as shown in Figure 4d,e, the set/reset voltage and on/off ratio of Pt/Al_2O_3/Ta/Pt memristors are increased with the increase in Al_2O_3 deposition temperature. Figure 4f shows the resistance distribution of the Pt/Al_2O_3/Ta/Pt memristors that have different Al_2O_3 deposition temperatures at both on and off states in the pulse switching measurements. It is noticeable that the variation of different memristors is different, and the Pt/120 °C-deposited Al_2O_3/Ta/Pt memristor has the lowest variation. All of these demonstrate that the Al_2O_3 deposition temperature directly affects the characteristics of the Pt/Al_2O_3/Ta/Pt memristor. In other words, the characteristics of the Pt/Al_2O_3/Ta/Pt memristor can be modified specifically by controlling the crystallinity of the switching layer material (Al_2O_3).

Different crystalline Al_2O_3 has different grain sizes. In order to understand the effect of the switching layer material (Al_2O_3) crystallinity on the memristor characteristics at the atomic level, multimillion-atom molecular dynamic simulations of the active Al_2O_3 layer with different grain sizes were performed. As mentioned in Table 1, the estimated average grain size of the polycrystalline Al_2O_3 deposited at 160 and 200 °C is ∼150.5 and ∼207.0 nm, respectively. Because of the simulation resource limitation, it is really hard to do MD simulation for polycrystalline Al_2O_3 films that have these grain sizes. Because we just want to study the effect of crystallinity qualitatively, we change the simulation cell to Al_2O_3 layers that are amorphous and with grain sizes at 2, 4, and 50 nm and were studied numerically. They were chosen to present Al_2O_3 films that are amorphous, in transition between amorphous and polycrystalline and polycrystalline. Figure 5a−d shows the constructed amorphous Al_2O_3 layer using a melt-quench scheme[38] and the constructed microstructures of Al_2O_3 layers at grain sizes of 2, 4, and 50 nm using a Voronoi-annealing scheme,[39−41]

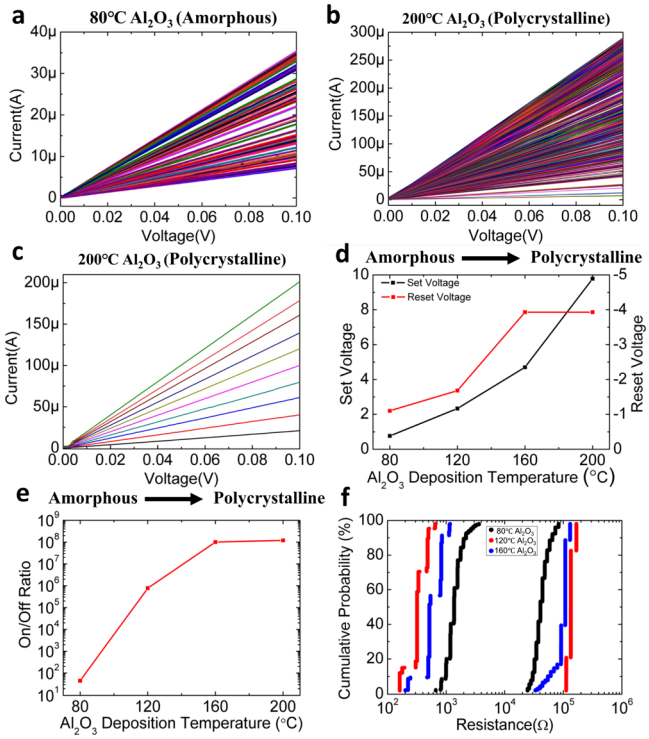


Figure 4. Modifying Pt/Al_2O_3/Ta/Pt memristor characteristics through controlling the switching layer material (Al_2O_3) crystallinity. (a) Our memristor can be set to different conductance states using different compliance currents. Here, the $I-V$ curves for the Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor with different conductances are shown, which has 31 states (around 2^5). (b) $I-V$ curves for the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor with different conductances, which has 314 states (more than 2^8). (c) Through controlling the compliance currents, our memristor can be set to the target conductance state precisely. Here, the ten set conductance states (200, 400, 600, 800, 1000, 1200, 1400, 1600, 1800, and 2000 μS) of the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor are shown. (d) Change of the set/reset voltage of the Pt/Al_2O_3/Ta/Pt memristor with respect to the Al_2O_3 deposition temperature. (e) Change of the on/off ratio of the Pt/Al_2O_3/Ta/Pt memristor with respect to the Al_2O_3 deposition temperature. The on/off ratios are calculated at read voltage 0.3 V according to Figure 3a. (f) Resistance distribution (2 to 98%) of the Pt/Al_2O_3/Ta/Pt memristors that have different Al_2O_3 deposition temperatures at both on and off states in the pulse switching measurements (Figure 3e−g).

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537

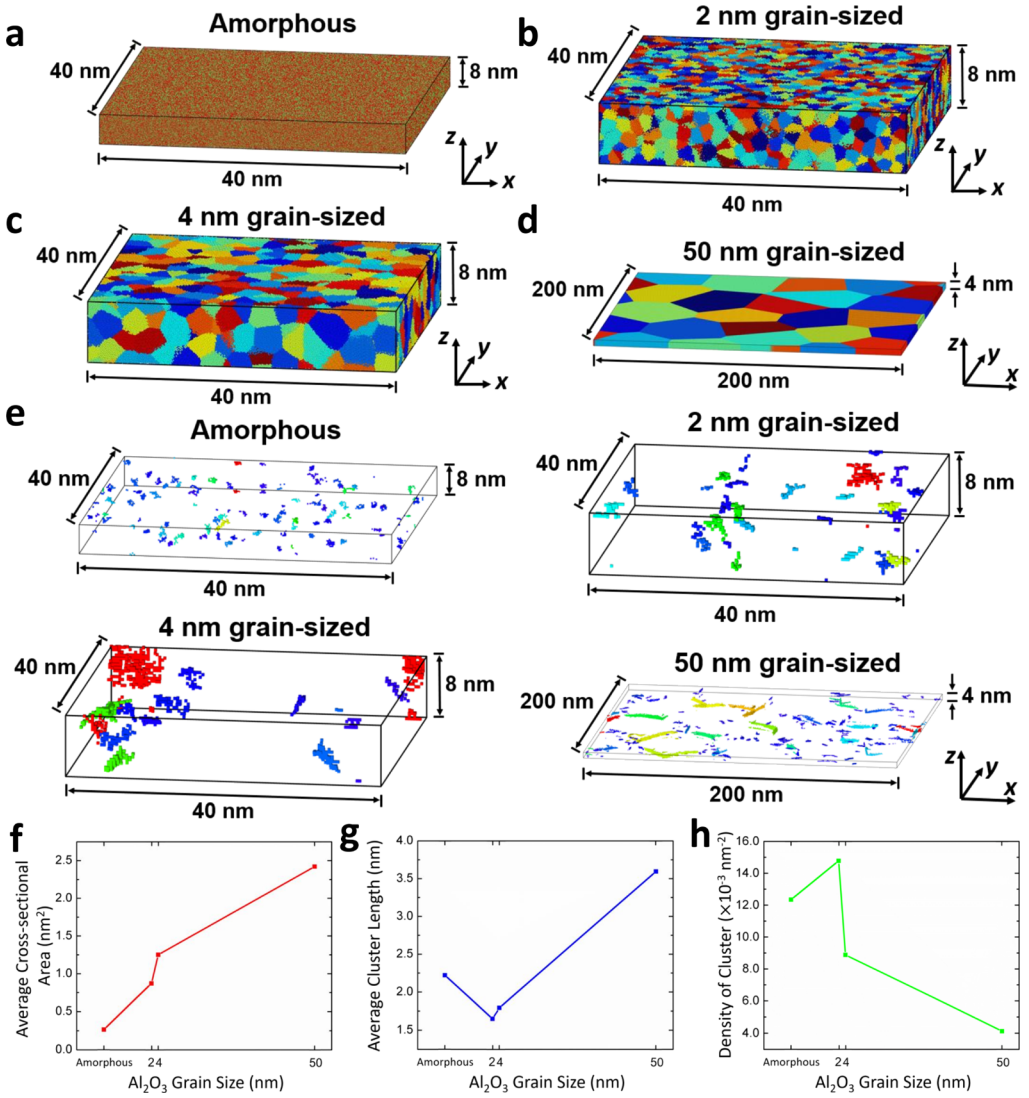


Figure 5. Working mechanism study. (a) Microstructure of the amorphous Al_2O_3 layer generated by a melt-quench scheme. (b) Microstructures of 2 nm grain-sized Al_2O_3 layer generated using the Voronoi-annealing scheme. (c) Microstructures of the 4 nm grain-sized Al_2O_3 layer generated using the Voronoi-annealing scheme. (d) Microstructures of the 50 nm grain-sized Al_2O_3 layer generated using the Voronoi-annealing scheme. (e) Connected clusters of low-density voxels in different Al_2O_3 layers identified using a depth first search (DFS) method. Connected clusters in each layer are denoted by different colors for clarity. (f) Average cross-sectional area (in the $x-y$ plane) for each cluster of low-density voxels with respect to the Al_2O_3 layer type. (g) Average length of low-density voxels cluster with respect to the Al_2O_3 layer type. 50 nm grain-sized Al_2O_3 structures with larger grain sizes containing low-density clusters of the longest length (along the z direction). (h) Density of low-density voxel clusters with respect to the Al_2O_3 layer type. Amorphous and small grained structures have a significantly larger number density of connected voxel clusters than larger grain-sized structures.

respectively (details can be found in the Molecular Dynamics Simulations of Methods section).

The characteristics of $Pt/Al_2O_3/Ta/Pt$ memristors are determined by the energetics of formation and dissolution of conductive filaments.[15,42,43] In addition, the grain boundaries of the Al_2O_3 layer and regions of a low local atomic density in the Al_2O_3 layer constitute potential pathways for the formation of conductive filaments in the $Pt/Al_2O_3/Ta/Pt$ memristors.[44−49] As a result, the characteristics of $Pt/Al_2O_3/Ta/Pt$ memristors can be estimated by quantifying the dimension and connectivity of grain boundaries and regions of a low local atomic density in the Al_2O_3 layer. To quantify this, a connected component analysis (using DFS) of low-density voxels was performed[50] (details can be found in the Molecular Dynamics Simulations of Methods section). Here, the low-density voxels are the 3 Å × 3 Å × 3 Å regions containing no Al or O atoms. Connected component analysis identifies all possible pathways for the conductive filaments. Figure 5e shows the results of the connected component analysis on different (amorphous, 2 nm grain-sized, 4 nm grain-sized, and 50 nm grain-sized) Al_2O_3 layers highlighting the structure and connectivity of local low-density voxels. The connected component analysis results indicate that the amorphous Al_2O_3 layer has a uniform distribution of small clusters of connected low-density voxels. In contrast, clusters of connected low-density voxels in other (2 nm grain-sized, 4 nm grain-sized, and 50 nm grain-sized) Al_2O_3 layers are more heterogeneously distributed and exist exclusively at the grain boundaries. Figure 5e also shows that nonamorphous Al_2O_3 layers can only form filaments through those low-density clusters on the grain boundary. This indicates that the characteristics of $Pt/Al_2O_3/Ta/Pt$ memristors using nonamorphous Al_2O_3 layers are mainly

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537

determined by the grain boundaries of the Al_2O_3 layer while not the regions of the low local atomic density in the Al_2O_3 layer. For Pt/Al_2O_3/Ta/Pt memristor nonamorphous Al_2O_3 layers, their characteristics are mainly determined by the regions of the low local atomic density in the Al_2O_3 layer. This is because that amorphous Al_2O_3 layers do not have grain boundaries.

It is reasonable to expect that the number of conductance states will be proportional to the cross-sectional area (in the $x-y$ plane) of the connected clusters of low-density voxels. This is because the larger cross-sectional area of the connected clusters of low-density voxels means more possible diameters of conductive filaments in memristors. Different conduction filament diameters correspond to different conductance states. Figure 5f shows the change in the cross-sectional area (in the $x-y$ plane) of the connected clusters of low-density voxels with respect to the type of Al_2O_3 layer. The cross-sectional area of the connected clusters increases from an amorphous to a polycrystalline Al_2O_3 layer, and further monotonically increases with the grain size. This behavior is consistent with the experimental observation of the number of resistance states of the Pt/80 °C-deposited Al_2O_3/Ta/Pt memristor and the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor (Figure 4a,b).

Figure 5g,h indicates that a large grain-sized Al_2O_3 layer has fewer but longer low-density clusters, while amorphous and small-grained Al_2O_3 layers contain a larger number of nonpercolating clusters of smaller lengths. As mentioned above, the characteristics of Pt/Al_2O_3/Ta/Pt memristors are determined by the energetics of formation and dissolution of conductive filaments. Both grain boundaries and regions of the low local atomic density in the Al_2O_3 layer constitute potential pathways for the formation of conductive filaments in the Pt/Al_2O_3/Ta/Pt memristors. As mentioned above, only amorphous Al_2O_3 layers have uniform distributions of small clusters of connected low-density voxels for filament formation, while nonamorphous Al_2O_3 layers can only form filaments through those low-density clusters on the grain boundary. That is why amorphous Al_2O_3 layers have the lowest programming voltage. Figure 5g,h also indicates that the larger grain-sized Al_2O_3 layer has fewer but longer low-density clusters for filament formation. The longer the cluster, the larger the programming voltage is needed. These results are consistent with the experimental results (Figure 3a–e). Moreover, as shown in Figure 3h, it is hard to switch the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor using pulse. This is because the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor needs the highest programming voltage. The larger the energy dumped on the memristor when it is switched on, the more the stress on the memristor. Therefore, the Pt/200 °C-deposited Al_2O_3/Ta/Pt memristor has the worst endurance. To be emphasized, these memristors are not damaged, they only need to be either reformed or to be used at different pulse parameters. In addition, the increase of conductive pathways (proportional to the density of low-density clusters) in the Al_2O_3 layer will reduce the variation in the electrical measurements of memristors. This is because that larger number of conductive pathways can decrease the effects of abnormal switching. If the density of low-density clusters in the Al_2O_3 layer is higher, the corresponding Pt/Al_2O_3/Ta/Pt memristor will have lower variation. This also fits the experimental results (Figures 3e–h and Figure 4f).

3. CONCLUSIONS

In summary, this work proposes and demonstrates a method to modify the memristor characteristics specifically by controlling the crystallinity of the switching layer material. By setting the ALD temperature, the crystallinity of the deposited Al_2O_3 can be controlled. Using different crystalline Al_2O_3 as the memristor switching layer, the characteristics of the corresponding Pt/Al_2O_3/Ta/Pt cross-point memristors can be engineered. When memristors are used as switches, the switching layer deposited at the highest "amorphous" temperature is preferred. When memristors are used to implement synapse-form neuromorphic computing, the switching layer deposited at higher temperature and polycrystalline film with a larger grain size is preferred. Good characteristics such as high I-V linearity, high on/off ratio (around 10^8), low pulse operation voltage (2.5 V), and multilevel conductance states (314 states) were obtained from our modified Pt/Al_2O_3/Ta/Pt memristors. More importantly, molecular dynamic simulations were performed to qualitatively study how the switching layer crystallinity affects the characteristics of memristors. We anticipate that through modifying the characteristics of memristors preciously, memristors can be used for a broad spectrum of applications in the near future.

4. METHODS

4.1. Device Fabrication. As shown in Figure 1a, first, a layer of 150 nm SiO_2 film was grown onto a 3-inch Si wafer (⟨100⟩) by thermal oxidation in a furnace (Thermco Products Corporation, MB71). Next, a lift-off layer (Shipley Microposit LOL 2000, 3000 rpm spin coating for 60 s and baking at 170 °C for 10 min) and a photoresist layer (AZ MiR 701, 3000 rpm spin coating for 40 s and baking at 90 °C for 1 min) was deposited onto the substrate. UV light exposure was performed at 54.3 mJ/cm^2 with a custom-designed photomask. Afterward, postbaking was performed at 110 °C for 1 min, and the substrate was immersed into the developer solution (AZ 300 MIF Developer) for 1 min. Then, 2 nm Ti (adhesion layer) and 20 nm Pt (bottom electrode metal) were vertically deposited onto the substrate by e-beam evaporation (Temescal BJD 1800 E-Beam Evaporator) with a deposition rate of 0.3 Å/s. Next, a lift-off process was performed by immersing the substrate into an acetone solution with ultrasound vibration and spraying the substrate with the acetone solution. The substrate was then immersed into the developer solution (AZ 300 MIF Developer) for 90 s to remove the residual lift-off layer. The patterns after the lift-off process consist of bottom electrodes. The samples were then covered with an 8 nm Al_2O_3 blanket layer using a plasma-enhanced ALD process (Oxford PlasmaPro 100). The ALD temperature can be set precisely to control the crystallinity of the deposited Al_2O_3. Finally, 8 nm thick Ta and a 20 nm thick Pt top electrode were defined using a second photolithography, evaporation, and lift-off process using the same recipes to get the Pt/Al_2O_3/Ta/Pt cross-point memristor.

4.2. Measurement and Characterization. The refractive index of Al_2O_3 deposited at different temperatures was measured by ellipsometry (Spectroscopic Ellipsometers, J.A. Woollam Co., Inc.). The high-resolution TEM images were acquired in a transmission electron microscope (Model: FEI Titan Themis G2 with spherical aberration and 4 detectors) operated at 200 keV. The cross-section samples were prepared with dual beam FIB (Model: FEI Helios 450S). The optical microscope image was taken with a Nikon Eclipse LV150N microscope. DC electrical characterizations, retention tests, pulse measurements, and multilevel conductance state measurements were all carried out with the Keithley 4200 semiconductor characterization system. The DC sweep rate is approximately 1 V/s. For the pulse measurements, the devices were programmed to on or off states, and the resistance was read at 1 V, 2 μs pulse between switching events. The retention tests at 85 °C were performed on a hot plate in the nitrogen environment.

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529–1537

4.3. Molecular Dynamics Simulation. An amorphous Al_2O_3 layer was prepared by the melt-quench scheme,[38] that is, by cooling the melt. Starting from a crystalline α-Al_2O_3, the system was gradually heated until a very well-thermalized, high temperature liquid at 3000 K was obtained. From this liquid, the system was gradually cooled to 300 K in a total of 50 ps and was thermalized for 700 ps.

The nanocrystalline α-Al_2O_3 layers were generated using the Voronoi tessellation method.[39−41] Three layers were generated with 2, 4, and 50 nm average grain size. The 2 and 4 nm grain size layers are three-dimensional nanostructures with grain distributed in a 40 × 40 × 8 nm periodic cell. The 50 nm grain size layer is a two-dimensional nanostructure with columnar grains distributed in a 200 × 200 × 4 nm cell. The centers for the tessellations are randomly distributed points within the sample with points closer than 0.4 d removed to avoid producing grains with very large aspect ratios. Once the grain microstructure was obtained, the atomic positions were chosen by randomly assigning a crystallographic orientation to each grain and then placing atoms on sites of the appropriately oriented α-Al_2O_3 lattice. Periodic boundary conditions were applied in all three directions. The α-Al_2O_3 nanocrystals were annealed to eliminate low- or high-density regions near the GB and triple junctions. Annealing was also used to relax the GB structure and residual stresses. The annealing process was done by increasing the temperature of the sample to 2000 K for 20 ps. Samples were further relaxed at 100 K and P = 0 GPa for a further 20 ps.

DFS is an algorithm to traverse the tree or graph.[50] DFS was employed to identify all possible Ta diffusion pathways in the Al_2O_3 layer. Because diffusion of Ta in alumina can occur only through the low-density regions, a graph of the low-density region was created to be used in DFS search, using the following steps. After thermalization, the molecular dynamics system was divided into a voxel of size 27 $Å^3$. Each voxel with no aluminum or oxygen atoms is called empty voxel and treated as a node on the graph. Further, if the nearest voxel of each is empty, an edge between both nodes will be created. DFS was performed on the graph to identify all the connected paths in the graphs. Each path found by DFS empty voxels will allow the transfer of Ta in the Al_2O_3 layer.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.0c00148.

HAADF STEM and EDS images of the deposited Al_2O_3 film; I−V curves of multiple switching cycles of the Pt/Al_2O_3/Ta/Pt memristor; more pulse switching data of the Pt/Al_2O_3/Ta/Pt memristor from different devices; and repeatability and stability of multilevel conductance states of Pt/Al_2O_3/Ta/Pt memristors (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Wei Wu − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0001-6404-0317; Email: wu.w@usc.edu

Authors

Hao Yang − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0002-0992-9161

Buyun Chen − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Boxiang Song − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0002-4946-2738

Deming Meng − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Subodh Tiwari − *Collaboratory for Advanced Computing and Simulations, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0002-5516-6900

Aravind Krishnamoorthy − *Collaboratory for Advanced Computing and Simulations, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0001-6778-2471

Xiaodong Yan − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Zerui Liu − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Yunxiang Wang − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Pan Hu − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Tse-Hsien Ou − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0002-0892-908X

Paulo Branicio − *Collaboratory for Advanced Computing and Simulations, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0002-8676-3644

Rajiv Kalia − *Collaboratory for Advanced Computing and Simulations, University of Southern California, Los Angeles, California 90089, United States*

Aiichiro Nakano − *Collaboratory for Advanced Computing and Simulations, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0003-3228-3896

Priya Vashishta − *Collaboratory for Advanced Computing and Simulations, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0003-4683-429X

Fanxin Liu − *Collaborative Innovation Center for Information Technology in Biological and Medical Physics, and College of Science, Zhejiang University of Technology, Hangzhou, Zhejiang 310023, China*

Han Wang − *Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0001-5121-3362

Complete contact information is available at: https://pubs.acs.org/10.1021/acsaelm.0c00148

Author Contributions

H.Y. and B.C. contributed equally to this work. H.Y., B.C., B.S., and W.W. designed the experiments. H.Y., B.C., B.S., D.M., and W.W. performed the fabrication and material characterizations. S.T., A.K., P.B., R.K., A.N., and P.V. performed the simulation. H.Y., B.C., B.S., Z.L., Y.W., P.H., T.O., and W.W. performed the analyses. B.C., Y.X., and H.W. performed the

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537

electrical characterizations. F.L. was responsible for taking TEM images. W.W. supervised the work. H.Y., B.C., B.S., S.T., A.K., A.N., and W.W. composed the manuscript. All of the authors reviewed and commented on the manuscript.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The fabrications were performed at the Keck Photonics Center, University of Southern California. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of AFRL or its contractors. This work was partially funded under AFRL's Conduction Channel Engineering in Memristor for Synapse contract, which was started in June 2019 and will continue through May 2022 (Grant Number FA-8750-19-1-0503). Simulation work was supported by the U.S. Department of Energy, Office of Science, Basic Energy Sciences, Materials Science and Engineering Division, Grant DE-SC0018195.

■ REFERENCES

(1) Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. The missing memristor found. *Nature* **2008**, *453*, 80.
(2) Kim, K. M.; Zhang, J.; Graves, C.; Yang, J. J.; Choi, B. J.; Hwang, C. S.; Li, Z.; Williams, R. S. Low-power, self-rectifying, and forming-free memristor with an asymmetric programing voltage for a high-density crossbar application. *Nano Lett.* **2016**, *16*, 6724−6732.
(3) Kumar, S.; Wang, Z.; Huang, X.; Kumari, N.; Davila, N.; Strachan, J. P.; Vine, D.; Kilcoyne, A. L. D.; Nishi, Y.; Williams, R. S. Conduction channel formation and dissolution due to oxygen thermophoresis/diffusion in hafnium oxide memristors. *ACS Nano* **2016**, *10*, 11205−11210.
(4) Yi, W.; Savel'Ev, S. E.; Medeiros-Ribeiro, G.; Miao, F.; Zhang, M.-X.; Yang, J. J.; Bratkovsky, A. M.; Williams, R. S. Quantized conductance coincides with state instability and excess noise in tantalum oxide memristors. *Nat. Commun.* **2016**, *7*, 11142.
(5) Ascoli, A.; Tetzlaff, R.; Chua, L.; Yi, W.; Williams, R. Memristor emulators: A note on modeling. *Advances in Memristors, Memristive Devices and Systems*; Springer, 2017; pp 1−17.
(6) Pi, S.; Li, C.; Jiang, H.; Xia, W.; Xin, H.; Yang, J. J.; Xia, Q. Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension. *Nat. Nanotechnol.* **2019**, *14*, 35.
(7) Zhou, Y.; Zhang, M.; Guo, Z.; Miao, L.; Han, S.-T.; Wang, Z.; Zhang, X.; Zhang, H.; Peng, Z. Recent advances in black phosphorus-based photonics, electronics, sensors and energy devices. *Mater. Horiz.* **2017**, *4*, 997−1019.
(8) Zhang, L.; Gong, T.; Wang, H.; Guo, Z.; Zhang, H. Memristive devices based on emerging two-dimensional materials beyond graphene. *Nanoscale* **2019**, *11*, 12413−12435.
(9) Yoon, J. H.; Wang, Z.; Kim, K. M.; Wu, H.; Ravichandran, V.; Xia, Q.; Hwang, C. S.; Yang, J. J. An artificial nociceptor based on a diffusive memristor. *Nat. Commun.* **2018**, *9*, 417.
(10) Zidan, M. A.; Jeong, Y.; Lee, J.; Chen, B.; Huang, S.; Kushner, M. J.; Lu, W. D. A general memristor-based partial differential equation solver. *Nat. Electron.* **2018**, *1*, 411.
(11) Xia, Q.; Robinett, W.; Cumbie, M. W.; Banerjee, N.; Cardinali, T. J.; Yang, J. J.; Wu, W.; Li, X.; Tong, W. M.; Strukov, D. B.; Snider, G. S.; Medeiros-Ribeiro, G.; Williams, R. S. Memristor− CMOS hybrid integrated circuits for reconfigurable logic. *Nano Lett.* **2009**, *9*, 3640−3645.
(12) Cai, F.; Correll, J. M.; Lee, S. H.; Lim, Y.; Bothra, V.; Zhang, Z.; Flynn, M. P.; Lu, W. D. A fully integrated reprogrammable memristor−CMOS system for efficient multiply−accumulate operations. *Nat. Electron.* **2019**, *2*, 290.
(13) Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; Chung, U.-I.; Yoo, I.-K.; Kim, K. A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta 2 O 5− x/TaO 2− x bilayer structures. *Nat. Mater.* **2011**, *10*, 625.
(14) Torrezan, A. C.; Strachan, J. P.; Medeiros-Ribeiro, G.; Williams, R. S. Sub-nanosecond switching of a tantalum oxide memristor. *Nanotechnology* **2011**, *22*, 485203.
(15) Jiang, H.; Han, L.; Lin, P.; Wang, Z.; Jang, M. H.; Wu, Q.; Barnell, M.; Yang, J. J.; Xin, H. L.; Xia, Q. Sub-10 nm Ta channel responsible for superior performance of a HfO 2 memristor. *Sci. Rep.* **2016**, *6*, 28525.
(16) Li, C.; Hu, M.; Li, Y.; Jiang, H.; Ge, N.; Montgomery, E.; Zhang, J.; Song, W.; Dávila, N.; Graves, C. E.; Li, Z.; Strachan, J. P.; Lin, P.; Wang, Z.; Barnell, M.; Wu, Q.; Williams, R. S.; Yang, J. J.; Xia, Q. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* **2018**, *1*, 52.
(17) Xia, Q.; Yang, J. J. Memristive crossbar arrays for brain-inspired computing. *Nat. Mater.* **2019**, *18*, 309.
(18) Li, C.; Wang, Z.; Rao, M.; Belkin, D.; Song, W.; Jiang, H.; Yan, P.; Li, Y.; Lin, P.; Hu, M.; Ge, N.; Strachan, J. P.; Barnell, M.; Wu, Q.; Williams, R. S.; Yang, J. J.; Xia, Q. Long short-term memory networks in memristor crossbar arrays. *Nat. Mach. Intell.* **2019**, *1*, 49.
(19) Zidan, M. A.; Strachan, J. P.; Lu, W. D. The future of electronics based on memristive systems. *Nat. Electron.* **2018**, *1*, 22.
(20) Ho, Y.; Huang, G. M.; Li, P. Nonvolatile memristor memory: device characteristics and design implications. *Proceedings of the 2009 International Conference on Computer-Aided Design*; ACM, 2009; pp 485−490.
(21) Jagtap, A. J. *The Memristor and its Applications in RAM and Logic Gates*; California State University: Long Beach, 2016.
(22) Cong, J.; Xiao, B. mrFPGA: A Novel FPGA Architecture with Memristor-Based Reconfiguration. *2011 IEEE/ACM International Symposium on Nanoscale Architectures*; IEEE, 2011; pp 1−8.
(23) Li, C.; Han, L.; Jiang, H.; Jang, M.-H.; Lin, P.; Wu, Q.; Barnell, M.; Yang, J. J.; Xin, H. L.; Xia, Q. Three-dimensional crossbar arrays of self-rectifying Si/SiO 2/Si memristors. *Nat. Commun.* **2017**, *8*, 15666.
(24) Wang, Z.; Joshi, S.; Savel'ev, S.; Song, W.; Midya, R.; Li, Y.; Rao, M.; Yan, P.; Asapu, S.; Zhuo, Y.; Jiang, H.; Lin, P.; Li, C.; Yoon, J. H.; Upadhyay, N. K.; Zhang, J.; Hu, M.; Strachan, J. P.; Barnell, M.; Wu, Q.; Wu, H.; Williams, R. S.; Xia, Q.; Yang, J. J. Fully memristive neural networks for pattern classification with unsupervised learning. *Nat. Electron.* **2018**, *1*, 137.
(25) Wang, Z.; Li, C.; Song, W.; Rao, M.; Belkin, D.; Li, Y.; Yan, P.; Jiang, H.; Lin, P.; Hu, M.; Strachan, J. P.; Ge, N.; Barnell, M.; Wu, Q.; Barto, A. G.; Qiu, Q.; Williams, R. S.; Xia, Q.; Yang, J. J. Reinforcement learning with analogue memristor arrays. *Nat. Electron.* **2019**, *2*, 115.
(26) Zhu, X.; Du, C.; Jeong, Y.; Lu, W. D. Emulation of synaptic metaplasticity in memristors. *Nanoscale* **2017**, *9*, 45−51.
(27) Bayat, F. M.; Prezioso, M.; Chakrabarti, B.; Nili, H.; Kataeva, I.; Strukov, D. Implementation of multilayer perceptron network with highly uniform passive memristive crossbar circuits. *Nat. Commun.* **2018**, *9*, 2331.
(28) Hu, M.; Graves, C. E.; Li, C.; Li, Y.; Ge, N.; Montgomery, E.; Davila, N.; Jiang, H.; Williams, R. S.; Yang, J. J.; Xia, Q.; Strachan, J. P. Memristor-based analog computation and neural network classification with a dot product engine. *Adv. Mater.* **2018**, *30*, 1705914.
(29) Jeong, Y.; Lee, J.; Moon, J.; Shin, J. H.; Lu, W. D. K-means data clustering with memristor networks. *Nano Lett.* **2018**, *18*, 4447−4453.
(30) Jeong, Y.; Lu, W. Neuromorphic computing using memristor crossbar networks: A focus on bio-inspired approaches. *IEEE Nanotechnol. Mag.* **2018**, *12*, 6−18.
(31) Yang, J. J.; Strukov, D. B.; Stewart, D. R. Memristive devices for computing. *Nat. Nanotechnol.* **2013**, *8*, 13.
(32) Puurunen, R. L. Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process. *J. Appl. Phys.* **2005**, *97*, 121301.

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537

(33) Miikkulainen, V.; Leskelä, M.; Ritala, M.; Puurunen, R. L. Crystallinity of inorganic films grown by atomic layer deposition: Overview and general trends. *J. Appl. Phys.* **2013**, *113*, 021301.
(34) Du, C.; Cai, F.; Zidan, M. A.; Ma, W.; Lee, S. H.; Lu, W. D. Reservoir computing using dynamic memristors for temporal information processing. *Nat. Commun.* **2017**, *8*, 2204.
(35) Jiang, H.; Belkin, D.; Savel'ev, S. E.; Lin, S.; Wang, Z.; Li, Y.; Joshi, S.; Midya, R.; Li, C.; Rao, M. A novel true random number generator based on a stochastic diffusive memristor. *Nat. Commun.* **2017**, *8*, 882.
(36) Kumar, S.; Strachan, J. P.; Williams, R. S. Chaotic dynamics in nanoscale NbO 2 Mott memristors for analogue computing. *Nature* **2017**, *548*, 318.
(37) Nili, H.; Adam, G. C.; Hoskins, B.; Prezioso, M.; Kim, J.; Mahmoodi, M. R.; Bayat, F. M.; Kavehei, O.; Strukov, D. B. Hardware-intrinsic security primitives enabled by analogue state and nonlinear conductance variations in integrated memristors. *Nat. Electron.* **2018**, *1*, 197.
(38) Vashishta, P.; Kalia, R. K.; Nakano, A.; Rino, J. P. Interaction potentials for alumina and molecular dynamics simulations of amorphous and liquid alumina. *J. Appl. Phys.* **2008**, *103*, 083504.
(39) Brostow, W.; Dussault, J.-P.; Fox, B. L. Construction of Voronoi polyhedra. *J. Comput. Phys.* **1978**, *29*, 81−92.
(40) Finney, J. L. A procedure for the construction of Voronoi polyhedra. *J. Comput. Phys.* **1979**, *32*, 137−143.
(41) Tanemura, M.; Ogawa, T.; Ogita, N. A new algorithm for three-dimensional Voronoi tessellation. *J. Comput. Phys.* **1983**, *51*, 191−207.
(42) Wang, Z.; Li, C.; Lin, P.; Rao, M.; Nie, Y.; Song, W.; Qiu, Q.; Li, Y.; Yan, P.; Strachan, J. P.; Ge, N.; McDonald, N.; Wu, Q.; Hu, M.; Wu, H.; Williams, R. S.; Xia, Q.; Yang, J. J. In situ training of feed-forward and recurrent convolutional memristor networks. *Nat. Mach. Intell.* **2019**, *1*, 434−442.
(43) Sun, W.; Gao, B.; Chi, M.; Xia, Q.; Yang, J. J.; Qian, H.; Wu, H. Understanding memristive switching via in situ characterization and device modeling. *Nat. Commun.* **2019**, *10*, 1−13.
(44) Mok, I.-S.; Kim, J.; Lee, K.; Kim, Y.; Sohn, H.; Kim, H. Effect of crystallinity on the resistive switching behavior of HfAlO x films. *J. Korean Phys. Soc.* **2014**, *64*, 419−423.
(45) Lin, C.-C.; Wu, Y.-H.; Hung, T.-H.; Hou, C.-Y. Impact of dielectric crystallinity on the resistive switching characteristics of ZrTiOx-based metal−insulator-metal devices. *Microelectron. Eng.* **2013**, *109*, 374−377.
(46) Lanza, M.; Bersuker, G.; Porti, M.; Miranda, E.; Nafría, M.; Aymerich, X. Resistive switching in hafnium dioxide layers: Local phenomenon at grain boundaries. *Appl. Phys. Lett.* **2012**, *101*, 193502.
(47) Park, S.-J.; Lee, J.-P.; Jang, J. S.; Rhu, H.; Yu, H.; You, B. Y.; Kim, C. S.; Kim, K. J.; Cho, Y. J.; Baik, S.; Lee, W. In situ control of oxygen vacancies in TiO2 by atomic layer deposition for resistive switching devicesr. *Nanotechnology* **2013**, *24*, 295202.
(48) Mähne, H.; Berger, L.; Martin, D.; Klemm, V.; Slesazeck, S.; Jakschik, S.; Rafaja, D.; Mikolajick, T. Filamentary resistive switching in amorphous and polycrystalline Nb2O5 thin films. *Solid-State Electron.* **2012**, *72*, 73−77.
(49) Clarke, H.; Brown, T.; Hu, J.; Ganguli, R.; Reed, A.; Voevodin, A.; Shamberger, P. J. Microstructure dependent filament forming kinetics in HfO2 programmable metallization cells. *Nanotechnology* **2016**, *27*, 425709.
(50) Tarjan, R. Depth-first search and linear graph algorithms. *SIAM J. Comput.* **1972**, *1*, 146−160.

https://dx.doi.org/10.1021/acsaelm.0c00148
ACS Appl. Electron. Mater. 2020, 2, 1529−1537